INT6400/INT1400 ⟩⟩⟩⟩InTellon®
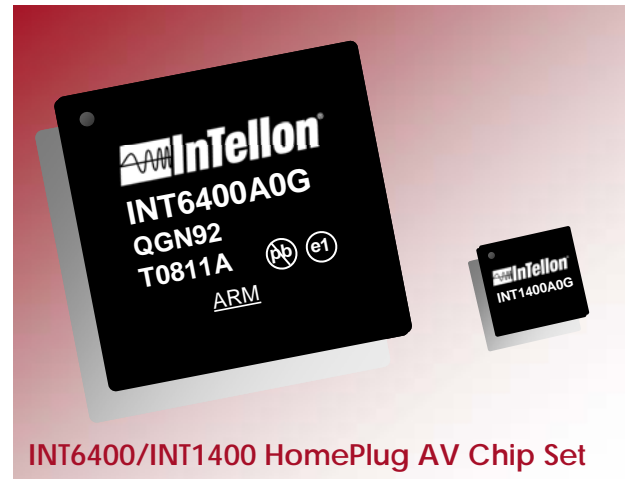## HomePlug AV Chip Set

NO NEW WIRES.

HomePlug® AV 200Mbps PHY

Features

INT6400

- HomePlug® AV MAC & PHY plus ADC and DAC in a 196-contact LBGA, Pb-free package

- MII (Host & PHY) interface

- Supports1024/256/64/16/8-QAM, QPSK, BPSK and ROBO Modulation Schemes

- 128-bit AES Link Encryption with key management for secure powerline communications

- Windowed OFDM with noise mitigation based on patented line synchronization techniques improves data integrity in noisy conditions

- Dynamic channel adaptation and channel estimation maximizes throughput in harsh channel conditions

- Advanced Turbo Code Forward Error Correction (*France Telecom – TDF – Groupe des écoles des télécommunications Turbo codes patents license*)

- HomePlug® AV MAC: TDMA and priority-based CSMA/CA channel access schemes

- ToS, CoS and IP Port Number Packet Classifiers

- Supports IGMP managed multicast sessions

- Green Standard (ROHS) Compliant

- Programmable-gain Rx/Tx

INT1400

- AFE/Line Driver IC

- Tx Filter, programmable-gain line driver, programmable-gain Rx amplifier

- Differential coupling

- 5 X 5 mm 32-pad QFN package

- Companion to INT6400

INT6400/INT1400 HomePlug AV Chip Set

Benefits

- **Third-generation HomePlug AV**

- **High-performance cost-down solution**

- **Two-chip set**

The Intellon INT6400/INT1400 HomePlug AV chip set solution is comprised of the INT6400 Medium Access Controller (MAC)/Physical layer (PHY) and INT1400 AFE/Line Driver ICs.

This Intellon HomePlug AV transceiver is optimized for multi-media streaming applications and is fully compliant with the HomePlug AV standard to reliably deliver up to 200 Mbps PHY rate over power line wiring.

The INT6400 includes a complete HomePlug-AV MAC and PHY, an Ethernet MII (media independent interface), an external SDRAM (synchronous dynamic random access memory) interface, along with interfaces for 2 external SPI (serial peripheral interface) devices. In addition, the INT6400 includes the A/D (analog-to-digital) and D/A (digital-to-analog) converters required for analog interface to the INT1400 AFE/Line Driver IC.

The INT1400 AFE/Line Drive IC includes a Tx filter, a programmable-gain line driver and a programmable-gain Rx amplifier. The programmability of these amplifiers opens up new and important signal optimization functionality.

Functional Diagram
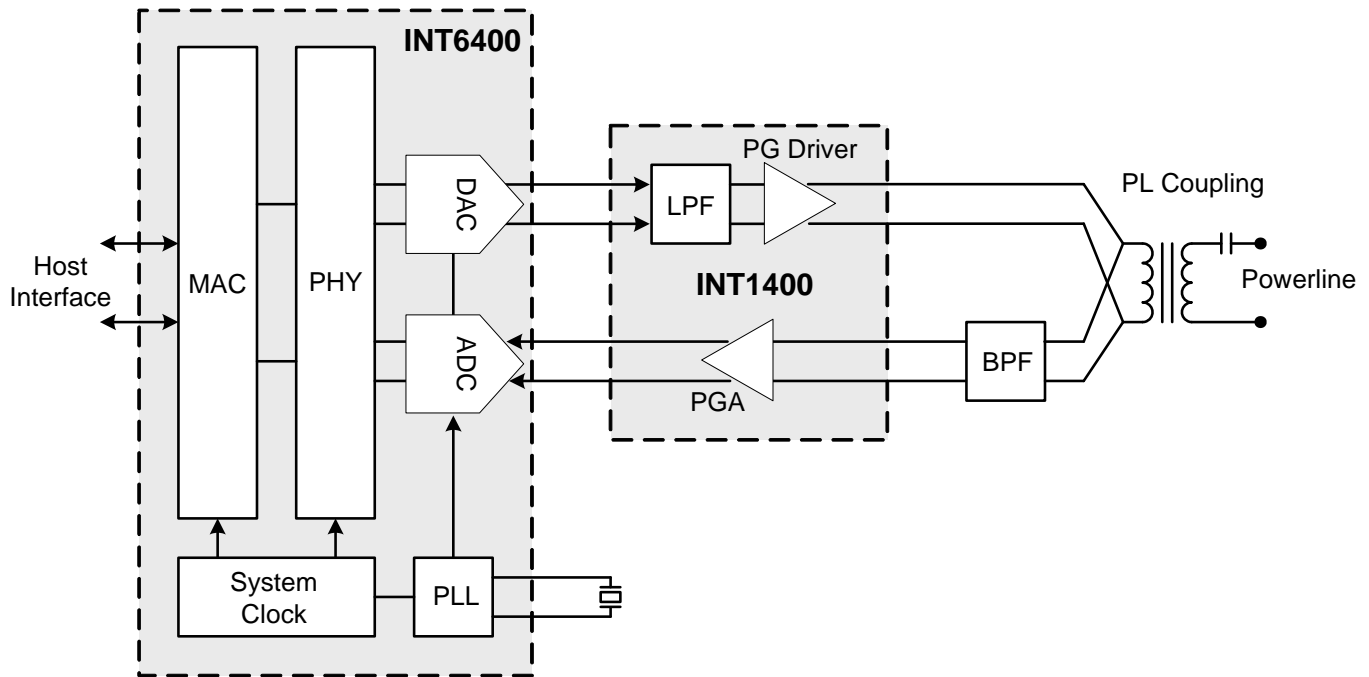
Within the INT6400, the HomePlug-AV MAC function is carried out by firmware running on an embedded ARM926EJ-S CPU (central processing unit), supported by DMA (direct memory access) hardware, two dedicated CRC (cyclic redundancy check) engines, and a large off-chip SDRAM data-store. The HomePlug-AV MAC firmware running on the CPU oversees operation of the integrated HomePlug-AV PHY via an interface that carries control/status information as well as transmits and receives data packets. General-purpose I/O pins are available to drive LEDs (light emitting diodes) directly to indicate link status, as well as to indicate user reset or network-attach events. An on-chip PLL (phase locked loop) and built-in crystal oscillator driver permit generation of system clocks from a single external 37.5 MHz crystal.

In addition to the processor, the MAC also contains numerous peripherals that are essential for running an advanced Real-Time Operating System (RTOS). The MAC contains a reset/clock controller, numerous timers, a vector interrupt controller, a synchronous and an asynchronous UART (universal asynchronous receiver transmitter), GPIO (general purpose input output) support, and a complex self-diagnostic module. These peripherals allow the RTOS and MAC software to respond to system interrupts, and control the operation of the software.

Numerous on-chip busses allow unimpeded access to critical system resources – most notably, the SDRAM interface and the small on-chip SRAM (Static Random Access Memory). The on-chip SRAM is used for storing time-critical descriptor chains, while the off-chip SDRAM is used for storing the majority of the descriptor information, as well as the packet data. The descriptor engine is responsible for moving data to and from memory (either on-chip SRAM or off-chip SDRAM), for merging packets together, and for providing status and interrupt information back to the processor. A key factor here is to reduce the number of interrupts that the processor must respond to – with the high data rates that are achievable through the HomePlug-AV PHY, it is essential that a large proportion of the DMA processing is off-loaded to these descriptor engines.

Within the INT1400 is the TX filter, programmable-gain line driver and the programmable-gain RX amplifier. The lowpass filter has a cutoff of 30 MHz. The RX PGA provides 60 dB of gain control range, in 2 dB increments. The TX PG Line Driver provides 30 dB of gain control range, in 2 dB increments.

INT6400 General Specifications

Physical

Parameter	Value	Description
Package Type	LBGA-196, Pb-Free	196 contact Low Profile Ball Grid Array, 15 X 15 array, 1mm ball pitch
Dimensions	15 mm X 15 mm	Chip package dimensions
Moisture Sensitive Level (MSL)	3	JEDEC standard level 3
Ball Composition	96.5Sn/3.0Ag/0.5Cu	Tin/Silver/Copper
Height	1.4 mm	Maximum height above seating plane
Operating Temp. Range (T_A)	0°C to 70°C	Safe package operating temperature range

Interfaces

| Type	Description
MII (Ethernet)	Host or PHY, IEEE 802.3u Media Independent Interface
SPI	Serial Peripheral Interface to read/write INT6400 configuration and firmware image stored in external flash memory
SDRAM	SDRAM memory controller operates at 75 MHz, 100 MHz, 112.5 MHz or 150 MHz with 16-bit data bus

Technologies

Type	Description
Windowed OFDM	Windowed Orthogonal Frequency Division Multiplexing – provides over 1,000 narrow-band carriers each of which can be independently turned off (30-dB notch) or modulated up to 1024 QAM for optimal performance
TDMA Channel Access	Time Division Multiple Access – a means of accommodating more than one service on the channel by assigning time slots – useful for ensuring Quality of Service (QoS) for video streams
CSMA/CA Channel Access	Carrier-Sense Multiple Access/Collision Avoidance – a means of sensing the presence of a carrier before transmission is attempted to avoid network collisions or contention

Performance

Parameter	Value	Description
Maximum PHY Rate	200 Mbps	Maximum PHY rate including payload and overhead
Modulation	1024/256/64/16/8 QAM, QPSK, BPSK, ROBO	Each OFDM sub carrier can be independently modulated to optimize throughput for operating conditions
Encryption	128 bit AES	Matches industry standard Advanced Encryption System

INT1400 General Specifications

Parameter	Value	Description
Package Type	QFN, Pb-Free	32-pad Quad Flat No-lead package
Dimensions	5 mm X 5 mm	Chip package dimensions
Moisture Sensitive Level (MSL)	3	JEDEC standard level 3
Pad Composition	96.5Sn/3.0Ag/0.5Cu	Tin/Silver/Copper
Height	1.4 mm	Maximum height above seating plane
Operating Temp. Range (T_A)	0°C to 70°C	Safe package operating temperature range
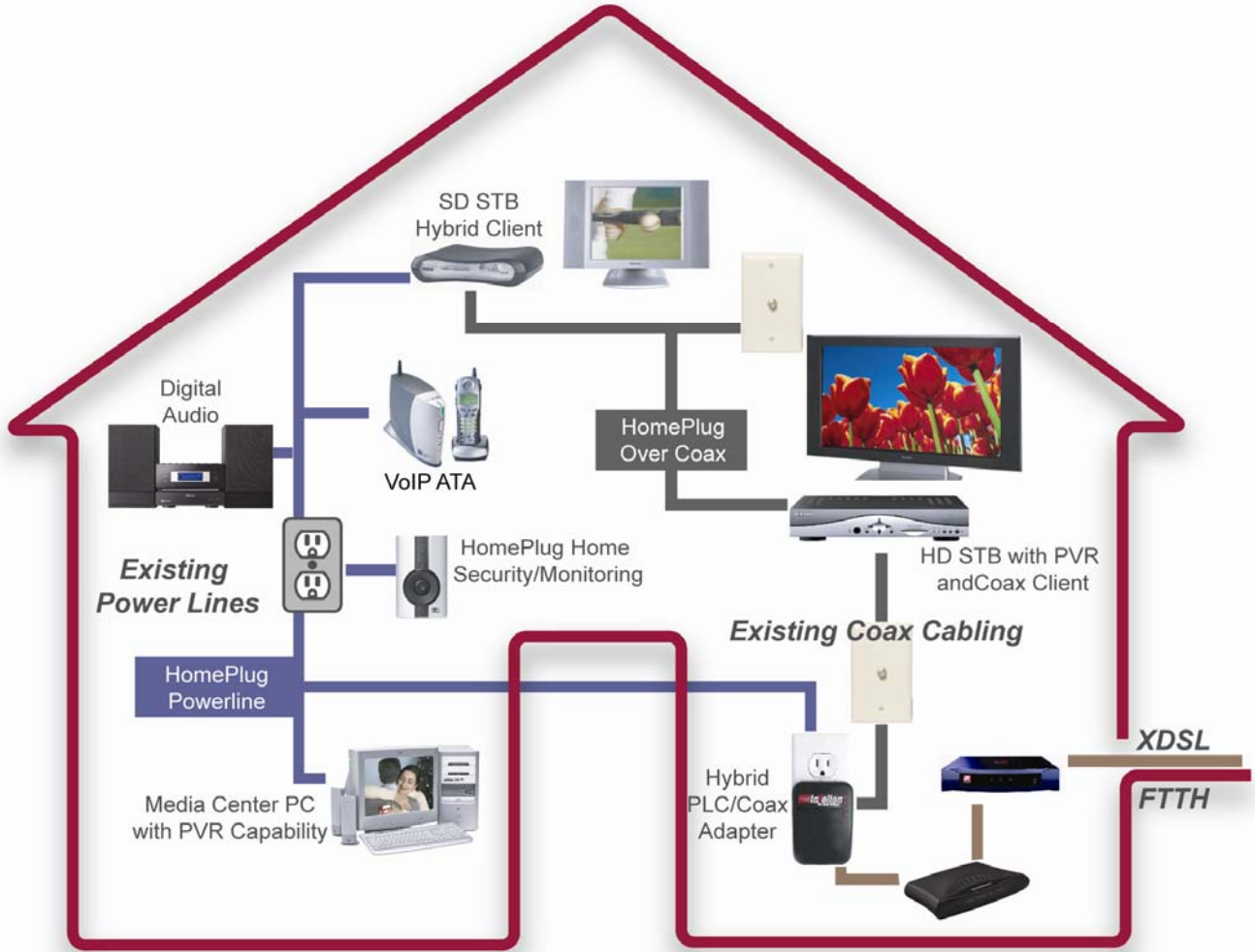
Ordering Information

INT6400TR, INT1400TR Intellon HomePlug AV Chip Set

InTellon®
NO NEW WIRES.

HOMEPLUG
POWERLINE ALLIANCE
Founding Member

Corporate Headquarters
5955 T.G. Lee Blvd.
Suite 600
Orlando, FL 32822
(407) 428-2800
(407) 428-2850 (Fax)

Ocala Office
5100 West Silver Springs Blvd.
Ocala, FL 34482
(352) 237-7416
(352) 237-7616 (Fax)

San Jose Office
1731 Technology Drive
Suite 560
San Jose, CA 95110
(408) 501-0320
(408) 501-0323 (Fax)

Toronto Office
144 Front Street West,
Suite 385
Toronto, Ontario M5J 2L7
(416) 217-0451
(416) 217-0459 (Fax)